AMENDMENTS TO THE CLAIMS

Please amend claims 1, 3, 6, 8, 11 and 13 as set forth below, without acquiescence in the Office Action's reasons for rejection or prejudice to pursue in a related application. Claims 2, 4-5, 7, 9-10, 12 and 14-15 are unchanged.

1. (Currently Amended) A method for determining a worst-case transition comprising:

determining at least a plurality of slews of output timing events for a the plurality of input timing events based on a timing model of a gate; and

selecting a worst-case input timing event from the plurality of input timing events based on at least the slews of the output timing events.

2. (Original) The method of claim 1, further comprising:

determining a plurality of gate delays for a plurality of input signals based on the timing model of the gate.

3. (Currently Amended) The method of claim 2, wherein selecting a worst-case input timing event worst delay further comprises:

selecting a worst delay based on the gate delays.

4. (Original) The method of claim 1, wherein the timing model comprises:

$$D_g = F(S_i, C),$$
$$T_O = Q(T_i, D_g);$$

where D_g is a gate delay, T_i is an input slew, L is a load of the gate, and T_o is an output slew.

5. (Original) The method of claim 1, wherein the timing model is a timing library format (TLF) model.

6. (Currently Amended) An apparatus for determining a worst case transition comprising:

means for determining at least a plurality of output slews for a the plurality of input signals based on a timing model of a gate; and

means for selecting a worst delay input signal from the plurality of input signals based on at least the output slews.

7. (Original) The apparatus of claim 6, further comprising:

means for determining a plurality of gate delays for a plurality of input signals based on the timing model of the gate.

8. (Currently Amended) The apparatus of claim 7, wherein said means for selecting a worst-case input timing event ~~worst delay~~ further comprises:

means for selecting a worst delay based on the gate delays.

9. (Original) The apparatus of claim 6, wherein the timing model comprises:

$$D_g = F(T_i, C),$$
$$T_O = Q(T_i, D_g);$$

where D_g is a gate delay, T_i is an input slew, L is a load of the gate, and T_o is an output slew.

10. (Original) The apparatus of claim 6, wherein the timing model is a timing library format (TLF) model.

11. (Currently Amended) A computer readable medium storing a computer program comprising instructions which, when executed by a processing system, cause the system to perform a method for determining a worst case transition, the method comprising:

determining at least a plurality of output slews for a ~~the~~ plurality of input signals based on a timing model of a gate; and

selecting a worst delay input signal from the plurality of input signals based on at least the output slews.

12. (Original) The medium of claim 11, further comprising instructions, which, when executed by the processing system, cause the system to perform the method for determining a worst case transition, the method further comprising:

determining a plurality of gate delays for a plurality of input signals based on the timing model of the gate.

13. (Currently Amended) The medium of claim 12, further comprising instructions, which, when executed by the processing system, cause the system to perform the method for determining a worst case transition, wherein selecting a <u>worst-case input timing event</u> ~~worst delay~~ further comprises:

selecting a worst delay based on the gate delays.

14. (Original) The medium of claim 11, wherein the timing model comprises:

$$D_g = F(T_i, C),$$
$$T_O = Q(T_i, D_g);$$

where D_g is a gate delay, T_i is an input slew, L is a load of the gate, and T_o is an output slew.

15. (Original) The medium of claim 11, wherein the timing model is a timing library format (TLF) model.